

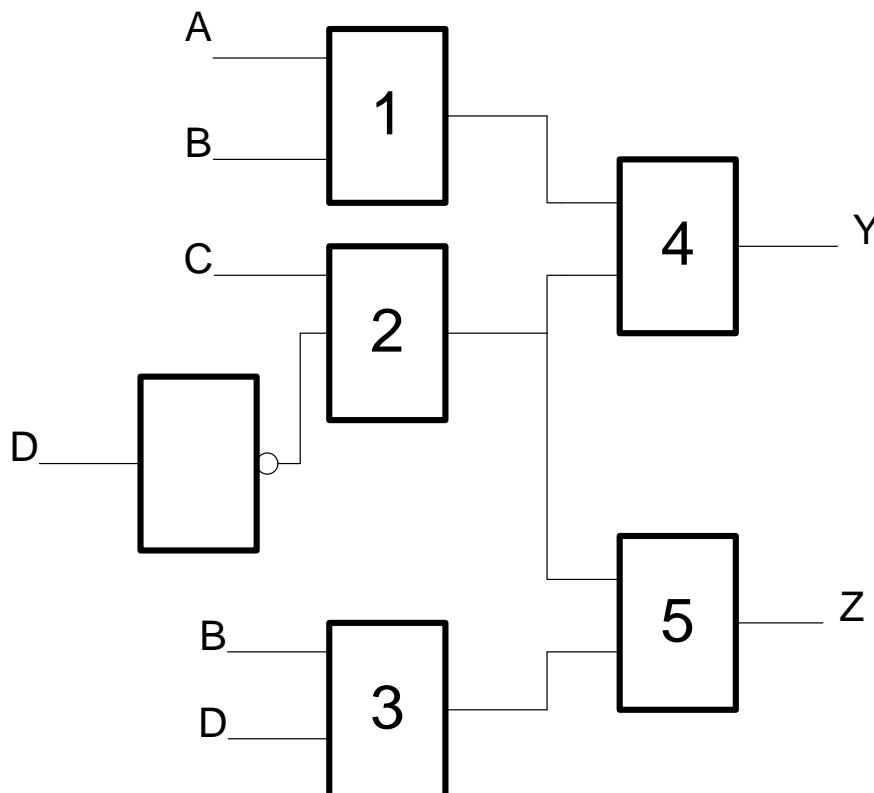
ANALYSIS OF COMBINATIONAL CIRCUITS

Layout 9: NOR – NOR – NOR – XNOR – XOR

Make analysis of a combinational circuit, the structure of which is given in the image.

1. From a known circuit structure:
 - Derive the Boolean functions corresponding with outputs Y and Z of circuit.
 - Boolean functions using the rules of Boolean algebra change on the minimum DNF and write it to Karnaugh maps (firstly to maps, where are all input variables of circuit and then to the smallest maps).
 - Boolean functions using the rules of Boolean algebra to change on the minimum KNF and write it to Karnaugh maps (firstly to maps, where are all input variables of circuit and then to the smallest maps).
2. Via system the LOGISIM (alt. LOG/FITBOARD):
 - Create the schema a given circuit and through the simulation to verify the accuracy of map entries of Boolean functions (different combinations of the input values to compare with the outputs values in the maps).
 - Create a schema of the equations, which were obtained when modification on the DNF.
 - Create a schema of the equations, which were obtained when modification on the KNF.
 - Connect properly all three schemes (use ramification from common inputs) and outputs of the circuits to place side by side (see. example of picture).

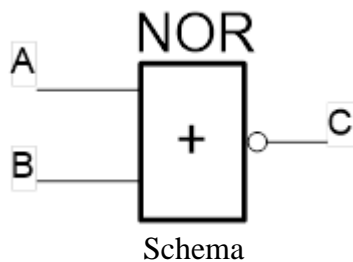
Schema of given circuit



1) The types of used logic gates: NOR – NOR – NOR – XNOR – XOR

NOR Function

$$C = \overline{A + B}$$

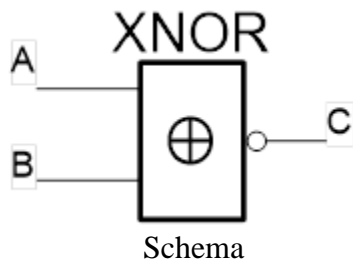


A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Table of truth values

XNOR Function

$$C = A.B + \overline{A}.\overline{B}$$

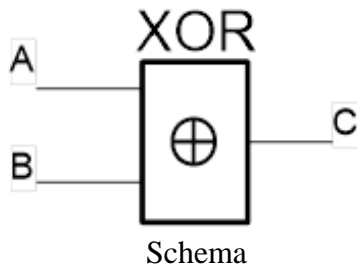


A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

Table of truth values

XOR Function

$$C = A.\overline{B} + \overline{A}.B$$



A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

Table of truth values

2) Based on the structure, we make the equations corresponding with outputs Y and Z:

$$Y = \overline{A+B} \cdot \overline{C+D} + \overline{A+B} \cdot \overline{C+D}$$

$$Z = \overline{C+D} \cdot \overline{B+D} + \overline{C+D} \cdot \overline{B+D}$$

3) We rewrite the equations to the equivalent normal form of type DNF:

Function Y:

$$Y = 1.2 + \overline{1}.\overline{2}$$

$$1 = \overline{A+B} =$$

$$= \overline{A} \cdot \overline{B}$$

De Morgan's law

$$2 = \overline{C+D} =$$

$$= \overline{C} \cdot \overline{D}$$

De Morgan's law

$$= \overline{C} \cdot D$$

Double negation

$$Y = 1.2 + \overline{1}.\overline{2}$$

$$= (\overline{A} \cdot \overline{B}) \cdot (\overline{C} \cdot D) + (\overline{A} \cdot \overline{B}) \cdot (\overline{C} \cdot \overline{D})$$

Substitutions of 1 and 2

$$= (\overline{A} \cdot \overline{B}) \cdot (\overline{C} \cdot D) + (\overline{A} + \overline{B}) \cdot (\overline{C} + \overline{D})$$

De Morgan's law

$$= (\overline{A} \cdot \overline{B}) \cdot (\overline{C} \cdot D) + (A+B) \cdot (C+\overline{D})$$

Double negation

$$= (\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot D) + (A \cdot C) + (A \cdot \overline{D}) + (B \cdot C) + (B \cdot \overline{D})$$

Distributivity

The number of used logic gates: 10 (4xNOT, 5xAND, 1xOR)

The number of inputs for logic function: 21 (1 to NOT, 1 to NOT, 1 to NOT, 1 to NOT, 4 to AND, 2 to AND, 2 to AND, 2 to AND, 2 to AND, 5 to OR)

Function Z:

$$Z = 2.\overline{3} + \overline{2}.3$$

$$2 = \overline{C+D} =$$

De Morgan's law

$$= \overline{C} \cdot \overline{D}$$

Double negation

$$\begin{aligned}
 &= \bar{C} \cdot D \\
 3 &= \overline{B + D} = && \text{De Morgan's law} \\
 &= \bar{B} \cdot \bar{D} \\
 Z &= 2 \cdot \bar{3} + \bar{2} \cdot 3 && \text{Substitutions of 2 and 3} \\
 &= (\bar{C} \cdot D) \cdot (\bar{B} \cdot \bar{D}) + (\bar{C} \cdot D) \cdot (\bar{B} \cdot \bar{D}) && \text{De Morgan's law} \\
 &= (\bar{C} \cdot D) \cdot (\bar{B} + \bar{D}) + (\bar{C} + \bar{D}) \cdot (\bar{B} \cdot \bar{D}) && \text{Double negation} \\
 &= (\bar{C} \cdot D) \cdot (B + D) + (C + \bar{D}) \cdot (\bar{B} \cdot \bar{D}) && \text{Distributivity} \\
 &= (\bar{C} \cdot B + \bar{C} \cdot D) \cdot (D \cdot B + D \cdot D) + (\bar{B} \cdot C + \bar{B} \cdot \bar{D}) \cdot (\bar{D} \cdot C + \bar{D} \cdot \bar{D}) && \text{Multiple equal inputs} \\
 &= (\bar{C} \cdot B + \bar{C} \cdot D) \cdot (D \cdot B + D) + (\bar{B} \cdot C + \bar{B} \cdot \bar{D}) \cdot (\bar{D} \cdot C + \bar{D}) && \text{Absorption} \\
 &= (\bar{C} \cdot B + \bar{C} \cdot D) \cdot (D) + (\bar{B} \cdot C + \bar{B} \cdot \bar{D}) \cdot (\bar{D}) && \text{Distributivity} \\
 &= (\bar{C} \cdot B \cdot D + \bar{C} \cdot D \cdot D) + (\bar{B} \cdot C \cdot \bar{D} + \bar{B} \cdot \bar{D} \cdot \bar{D}) && \text{Multiple equal inputs} \\
 &= (\bar{C} \cdot B \cdot D + \bar{C} \cdot D) + (\bar{B} \cdot C \cdot \bar{D} + \bar{B} \cdot \bar{D}) && \text{Distributivity} \\
 &= (\bar{C} \cdot D) \cdot (B + 1) + (\bar{B} \cdot \bar{D}) \cdot (C + 1) && \text{Annihilator for OR} \\
 &= (\bar{C} \cdot D) \cdot 1 + (\bar{B} \cdot \bar{D}) \cdot 1 \\
 &= \bar{C} \cdot D + \bar{B} \cdot \bar{D}
 \end{aligned}$$

The number of used logic gates: 6 (3xNOT, 2xAND, 1xOR)

The number of inputs for logic function: 9 (1 to NOT, 1 to NOT, 1 to NOT, 2 to AND, 2 to AND, 2 to OR)

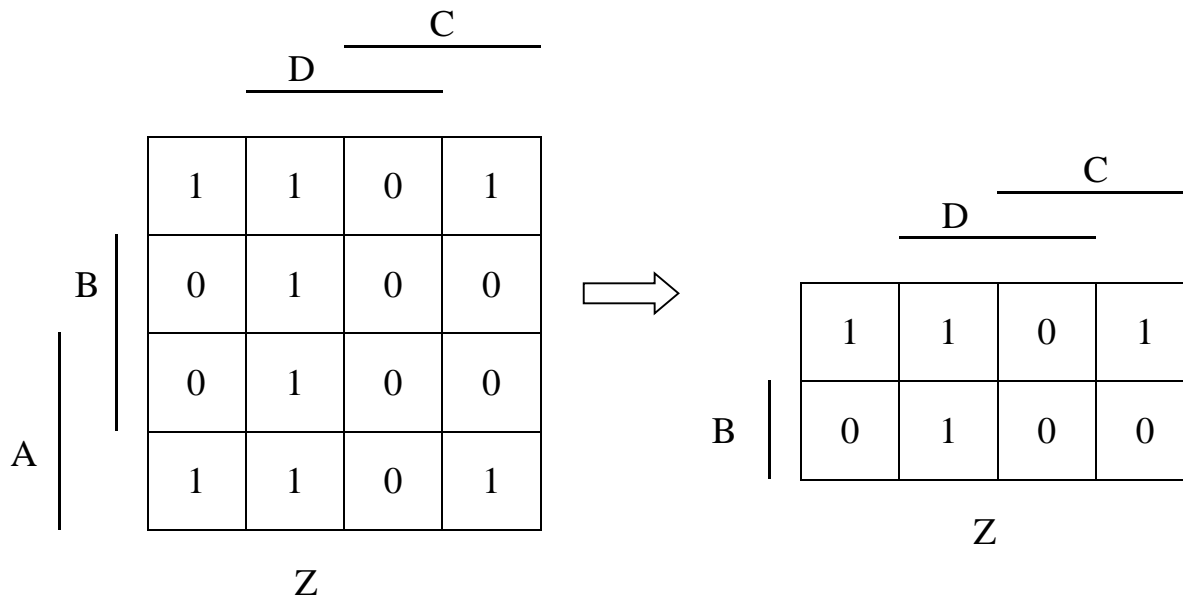
Summary of circuit:

The number of used logic gates: 13 (4xNOT, 7xAND, 2xOR)

The number of inputs for logic function: 24 (1 to NOT, 1 to NOT, 1 to NOT, 1 to NOT, 4 to AND, 2 to AND, 2 to AND, 2 to AND, 2 to AND, 2 to AND, 2 to OR, 2 to OR)

4) We compile maps of functions which correspond to expressions Y and Z:

		<u>C</u>			
		<u>D</u>			
A	B	0	1	0	0
		1	0	1	1
		1	0	1	1
		1	0	1	1
Y					



5) We rewrite the equations to the equivalent normal form of type KNF:

$$\begin{aligned}
 Y &= (\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D) + (A \cdot C) + (A \cdot \bar{D}) + (B \cdot C) + (B \cdot \bar{D}) && \text{Distributivity: (A) and (B)} \\
 &= (\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D) + A \cdot (C + \bar{D}) + B \cdot (C + \bar{D}) && \text{Distributivity: (C + } \bar{D}) \\
 &= (\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D) + (A + B) \cdot (C + \bar{D}) && \text{Rule 3a: } \underline{A}=(\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D), \underline{B}=(A + B), \underline{C}=(C + \bar{D}) \\
 &= ((\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D) + (A + B)) \cdot ((\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D) + (C + \bar{D})) && \text{Removing brackets} \\
 &= ((\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D) + A + B) \cdot ((\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot D) + C + \bar{D}) && \text{Rule 12a} \\
 &= ((\bar{C} \cdot D) + A + B) \cdot ((\bar{A} \cdot \bar{B}) + C + \bar{D}) && \text{Rule 3a. left side: } \underline{A}=(A + B), \text{ right side: } \underline{A}=(C + \bar{D}) \\
 &= (A + B + \bar{C}) \cdot (A + B + D) \cdot (\bar{A} + C + \bar{D}) \cdot (\bar{B} + C + \bar{D})
 \end{aligned}$$

The number of used logic gates: 7 (4xNOT, 1xAND, 4xOR)

The number of inputs for logic function: 20 (1 to NOT, 1 to NOT, 1 to NOT, 1 to NOT, 3 to OR, 3 to OR, 3 to OR, 3 to OR, 4 to AND)

$$\begin{aligned}
 Z &= \bar{C} \cdot D + \bar{B} \cdot \bar{D} && \text{Rule 3a (} \underline{A}=\bar{C} \cdot D) \\
 &= (\bar{C} \cdot D + \bar{B}) \cdot (\bar{C} \cdot D + \bar{D}) && \text{For first brackets we use Rule 3a} \\
 &= (\bar{C} + \bar{B}) \cdot (D + \bar{B}) \cdot (\bar{C} \cdot D + \bar{D}) && \text{For second brackets we use Rule 3a} \\
 &= (\bar{C} + \bar{B}) \cdot (D + \bar{B}) \cdot (\bar{C} + \bar{D}) \cdot (\bar{D} + D) && \text{For last brackets we use Rule 7a} \\
 &= (\bar{C} + \bar{B}) \cdot (D + \bar{B}) \cdot (\bar{C} + \bar{D}) \cdot (1) && \text{For first brackets we use Rule 9b} \\
 &= (\bar{B} + \bar{C}) \cdot (\bar{B} + D) \cdot (\bar{C} + \bar{D}) && \text{Consensus theorem} \\
 &= (\bar{B} + D) \cdot (\bar{C} + \bar{D})
 \end{aligned}$$

The number of used logic gates: 6 (3xNOT, 1xAND, 2xOR)

The number of inputs for logic function: 9 (1 to NOT, 1 to NOT, 1 to NOT, 2 to OR, 2 to OR, 2 to AND)

Summary of circuit:

The number of used logic gates: 8 (4xNOT, 2xAND, 6xOR)

The number of inputs for logic function: 26 (1 to NOT, 1 to NOT, 1 to NOT, 1 to NOT, 3 to OR, 3 to OR, 3 to OR, 3 to OR, 2 to OR, 2 to OR, 4 to AND, 2 to AND)

6) We compile maps of functions which correspond to expressions Y and Z:

		<u> C </u>			
		<u> D </u>			
A	B	0	1	0	0
	B	1	0	1	1
	B	1	0	1	1
	B	1	0	1	1

Y

		<u> C </u>			
		<u> D </u>			
A	B	1	1	0	1
	B	0	1	0	0
	B	0	1	0	0
	B	1	1	0	1

Z

⇒

		<u> C </u>			
		<u> D </u>			
B	B	1	1	0	1
	B	0	1	0	0

Z

Final assessment:

The first task was to derive the Boolean functions from known structure of the combinational logic circuit, which corresponding with outputs Y and Z. Then, to change functions to the minimum DNF, using the rules of Boolean algebra (mostly De Morgan's law and law about double negation). Such modified functions we had to write to the Karnaugh maps. On map for output "Z" may be seen that the variable "A" does not affect the output, so the map can be further reduced.

Similarly, the functions could be adjusted to a minimum DNF, according to the rules: distributivity (we used the substitution), rule about completeness or consensus theorem. This form of functions was entered to the Karnaugh maps and map for output "Z" could still be simplified by removing the variable "A".

Correctness of changed functions mDNF mKNF can be verified from their Karnaugh maps, which are identical with maps functions of a given combinational logic circuit.

Another task was to create a schemas for a given circuit, the circuit of equation DNF, the circuit of equation mKNF and all three circuits to connect on common inputs. By simulation we can verify the identity of outputs of all three circuits and values in the maps.

From the schema is clear that it is more convenient to use for the creation of circuit the equations KNF (whereby the logic circuit has 8 gates) as DNF (where it is needed 13 logic gates).

